WHAT IS CLAIMED IS:

1. A non-coherent frequency shift key demodulating circuit, comprising:

an oversampling device, for receiving and examining an input digital non-coherent frequency shift key signal carrying a digital signal upon existence of transition, and further outputting a data bit signal recording whether a transition exists or not;

a chain of registers, coupled to the oversampling device, receiving the data bit signal, and further counting and storing a quantity of logic high level status of the data bit signal received, and outputs a number-of-ones value signal correspondingly;

a threshold device, coupled to the chain of registers, for receiving and comparing the number-of-ones value signal with a predetermined threshold value to determine the digital signal carried in the input digital non-coherent frequency shift key signal.

2. The non-coherent frequency shift key demodulating circuit of claim **1**, wherein if the digital frequency shift key signal has a first frequency and a second frequency respectively representing a logic high level and a logic low level, the predetermined threshold value is determined as a quotient of a system data rate dividing a sum of the first frequency and the second frequency.

3. The non-coherent frequency shift key demodulating circuit of claim **1**, wherein the data bit signal is logic high level if a transition of the input digital non-coherent frequency shift key signal exists, and the data bit signal is logic low level if no transition of the incoming input digital non-coherent frequency shift key signal exists.

4. The non-coherent frequency shift key demodulating circuit of claim **1**, wherein the digital signal is determined a low level digital signal if a number-of-ones value signal is smaller than the predetermined threshold value, and the digital signal is

determined a high level digital signal if the number-of-ones value signal is higher than the predetermined threshold value.

5. A non-coherent frequency shift key demodulating method, comprises:

receiving and examining an input digital non-coherent frequency shift key signal carrying a digital signal upon existence of transition, and further outputting a data bit signal recording whether a transition exists or not;

receiving the data bit signal, and further counting and storing a quantity of logic high level status of the data bit signal received, and outputs a number-of-ones value signal correspondingly.

6. The non-coherent frequency shift key demodulating method as recited in claim **5**, wherein if the digital frequency shift key signal has a first frequency and a second frequency respectively representing a logic high level and a logic low level, the predetermined threshold value is determined as a quotient of a system data rate dividing a sum of the first frequency and the second frequency.

7. The non-coherent frequency shift key demodulating method as recited in claim **5**, wherein the data bit signal is logic high level if a transition of the input digital non-coherent frequency shift key signal exists, and the data bit signal is logic low level if no transition of the incoming input digital non-coherent frequency shift key signal exists.

8. The non-coherent frequency shift key demodulating method as recited in claim **5**, wherein the digital signal is determined a low level digital signal if a number-of-ones value signal is smaller than the predetermined threshold value, and the digital signal is determined a high level digital signal if the number-of-ones value signal is higher than the predetermined threshold value.